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Predictive Control for Reduced Structure Multilevel Converters: Experimenting on a Seven Level Packed U-Cell

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ABSTRACT

Recently, a branch of multilevel converters is emerged, in which their 'reduced structure' topologies use lower number of devices compared to the available topologies. To get a cost efficient converter, lower number of components as well as high quality waveforms, multilevel converters with a 'reduced structure' (MCRS) are suitable for high/medium power systems. Also, utilizing the fast microprocessors available today, applications of predictive control in power converters are of very powerful and attractive alternatives to classical controllers. This paper proposes a finite control set model-based predictive control (FCS-MPC) for load current regulation and capacitor voltage balancing for a typical MCRS. A case study considered, three-phase seven level packed U-cell (PUC), which is among reduced structure multilevel converters. A discrete model of the system is derived, and a predictive model-based control is developed according to this model in order to predict the future behavior of the system for all possible switching states; then, the switching state that optimized the cost function is selected. The feasibility of the proposed FCS-MPC strategy for a seven level PUC is evaluated based on simulations with MATLAB/ SIMULINK. Moreover, experimental validation of the proposed control system on a 5 kVA PUC is examined through DSP implementation**.**

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1. INTRODUCTION

Compared with conventional two level converters, multilevel converters can provide an efficient alternative to high power applications, providing a high quality output voltage, increasing the efficiency and robustness, and reducing the electromagnetic interference [1-2]. Energy efficiency, reliability, power density, simplicity, cost effectiveness, reduced structure with lower number of active and passive elements, high power quality, and application field are the main topics for distinguishing different topologies of multilevel converters [3]. Researchers all over the world are spending great efforts to introduce new topologies for multilevel converters [4-6]. Recently, a branch of multilevel converters is emerged, in which their 'reduced structure' topologies use lower number of devices compared to the available topologies [7-11]. To get a cost efficient converter, lower number of components as well as high quality waveforms, multilevel converters with a 'reduced structure' (MCRS) are suitable for high or medium power systems. In [12], a classification and review of MCRSs is presented. The conventional topologies are the basis for new researchers to develop a novel MCRS family of multilevel converters with lower number of power electronic devices. This paper considers the most recent 'multilevel converters' with a 'reduced structure' (MCRS).

Among different types of the MCRS, Packed U-cell (PUC) can be formed by manipulating either a conventional capacitor-clamped or the cascaded H-bridge multilevel topologies [13]. Each U-cell consists of

two power switches and one capacitor that produces more output voltage level using a small number of passive and active components. Low harmonic contents, more voltage levels in inverter output side, reduced filters rating, and possibility of combination of GTOs and IGBTs, are the main features of the PUC [13]. For the three phase PUC, the main disadvantage is the independent DC power supply for each phases. Also, the maximum phase voltage is limited to principal DC link voltage. Namely, maximum phase voltage is equal to the principal DC link amplitude.

Predictive control appears as an attractive alternative for the control of power converters and offers a number of advantages: no need for linear controllers and modulators, easy inclusion of nonlinearities and constraints, and fast dynamic response [14, 15]. Several control algorithms have been presented under the name of predictive control, as presented in [16]. Among these control schemes, finite control set model-based predictive control (FCS-MPC) has demonstrated to be a very powerful and attractive alternative for the control of power converters and have been used to implement different control strategies in power converter topologies and applications [17-22]. The basic idea of FCS-MPC is to predict the future behavior of the system based on its discrete model. Thereafter, the switching vector that optimizes a given cost function is selected and applied to the converter. The simultaneous control of the PUC output currents and DC-link capacitors voltages is done preferably with a model-based predictive controller (MBPC).

In this paper, essential steps for implementing the predictive control algorithm for a typical MCRS is presented. Thereafter, a discrete-time mathematical model of the three-phase PUC is derived and a predictive model-based control according to this discrete model is developed. This model is used to predict the future behavior of system for all possible switching state. The proposed predictive control strategy: 1) regulates the load currents; and 2) obtains capacitor voltage balancing of each phases. Performance of the proposed FCS-MPC strategy for a seven level packed U-cell converter is evaluated based on simulation studies in MATLAB/ SIMULINK software and experimental validation through real-time implementation on the DSP TMS320F28335.

This paper is organized as follows: in Section 2 essential steps for implementing FCS-MPC for a typical MCRS is presented; in Section 3 the PUC topology is introduced as a case study and its discrete model is derived; in Section 4 the theory of FCS-MPC is presented; and simulation and experimental results are presented in Section 5 and 6, respectively.

2. MODELING REDUCED STRUCTURE MULTILEVEL CONVERTERS

In this section, the essential steps for modeling of load and converter, and implementation of predictive controller will be presented. For implementing a predictive control based algorithm on a typical MCRS, the discrete mathematical model of the converter should be derived. According to this model, output voltage and capacitor voltages and currents should be calculated for each switching state of the converter. The key steps of this procedure that can be generalized for every discrete system, are summarized as follows:

- Deriving the discrete state space equations of the MCRSs.
- Obtaining the predictions, according to discrete mathematical model of MCRSs.
- Minimization of a predefined cost function.

It should be noted that, in this paper and for power converter application, a simple model of the inverter will be used (because of discrete nature and low switching frequency [17]). To illustrate the process, each step will be study separately as follows.

2.1. Discrete State Space Model of the Converter

Although various cost functions could be considered, only load current regulation and DC link capacitor voltage balancing is considered in this paper. By assuming that the plant is a typical MCRS (or other power converter), the discrete state space equations can be described by (in general form) [17]:

$$x_n(k+1) = A_1 x_n(k) + B_1 u(k)$$
$$y(k) = C_1 x_n(k) + D_1 u(k) \quad (1)$$

where u is the input variable (control actions or switching state vectors), y is the plant output (output voltage or current vectors), and x_n is the state space variable vector with dimension n_1.

The difference of the state-space equation is:

$$\Delta x_n(k+1) = A_1 \Delta x_n(k) + B_1 \Delta u(k) \quad (2)$$

To relate $\Delta x_n(k)$ to the output $y(k)$, a new state space variable vector is chosen to be [23]:

$$x(k) = [\Delta x_n(k)^T \quad y(k)]^T \quad (3)$$

where superscript T indicates matrix transpose.

Based on Equations (1), (2), and (3), the following state space model is derived (due to the principle of receding horizon control, $D_1 = 0$ in the discrete system model [23]):

$$x(k+1) = \boldsymbol{A}\, x(k) + \boldsymbol{B}\, \Delta u(k)$$
$$y(k) = \boldsymbol{C}x(k) \quad (4)$$

where

$$\boldsymbol{A} = \begin{bmatrix} A_1 & \overline{\boldsymbol{o}} \\ C_1A_1 & 1 \end{bmatrix}, \boldsymbol{B} = \begin{bmatrix} B_1 \\ C_1B_1 \end{bmatrix}, \boldsymbol{C} = [\overline{\boldsymbol{o}}\ \ 1], \overline{\boldsymbol{o}} = [0\ 0\ \dots\ 0]_{1\times n_1}$$

Based on the state space model (**A**, **B**, **C**), the future output variables are calculated as follows: (By assuming one-step-ahead prediction):

$$y(k+1) = \boldsymbol{CA}\, x(k) + \boldsymbol{CB}\, \Delta u(k) \quad (5)$$

According to Eqs. (4) and (5), for each input vector u (switching state vectors in power converter application), state space (capacitor voltage and load current) and output variables can be predicted.

2.2. Prediction of State Space Variables

After identifying all possible switching states of a typical MCRS, a specific voltage vector should be related to each switching states. Actually, each switching state vector generates a special voltage vector in AC side of the converter and as a result a look-up table is obtained. Also, a look-up table that determines the relation between flying capacitor and load currents is derived for each switching vector. So, there are two look-up tables that were used for prediction of state space variables. By using these look-up tables, measured and estimated parameters, flying capacitor voltages and load current can be calculated and predicted based on discrete state space model of the converter (Eqs. (4) and (5)). All the predicted control parameters inserted in a predefined cost function and optimized for selecting an appropriate switching state vector. These steps is summarized as follows:

- Identifying all possible switching state vectors of the considered MCRS.
- Relating each switching state to a specific voltage vector (look-up table 1).
- Relating flying capacitor currents to the load currents for each switching vector (look-up table 2).
- Capacitor voltage and load current measurement.
- Estimation of immeasurable parameters (such as internal voltage vector of the load).
- Prediction of state variables and future outputs of the system, based on state space model.
- Cost function optimization and selection of appropriate control action.

Based on discrete state space model of the system and by considering the capacitor voltage and load current vector as state variables, future behavior of the state variables can be derived. Namely, for all possible switching state, next sampling value of $x(k)$ should be calculated. For example, next sampling time value of flying capacitor voltage and load current vector can be written as:

$$v_c(k+1) = f(v_c(k), i_c(k))$$
$$\boldsymbol{i}(k+1) = f(\boldsymbol{i}(k), \boldsymbol{e}(k), \boldsymbol{v}(k)) \quad (6)$$

where $v_c(k)$ and $\boldsymbol{i}(k)$ are measured capacitor voltage and load current vector, respectively. Also, $i_c(k+1)$ (flying capacitor current) and $\boldsymbol{v}(k)$ (output voltage vector) should be derived from look-up tables 1 and 2. Finally, $\boldsymbol{e}(k)$ denotes internal voltage of a general load and estimated according to system equations.

2.3. Cost Function Optimization

The basic purpose of the predictive control system is to bring the predicted output $y(k)$ as close as possible to the reference signals $R_s(k)$. This objective is then translated into a cost function. There are different forms for cost functions. Considering fast sample periods, as is usual in power converters, different types of cost functions have same results [14]. Hence, the cost function g is calculated as presented by (7),

$$g = |R_s(k+1) - y(k+1)| \quad (7)$$

where $R_s(k)$ is a vector that contains the reference signals.

To find the optimal Δu (control action) that will minimize g, the below equation is used:

$$\frac{\partial g}{\partial \Delta u} = 0 \quad (8)$$

From which the optimal control signal Δu (switching state vector in power converter application) could be derived. Different tasks performed by the predictive control algorithm, is shown in Figure 1.

3. PACKED U-CELL CONVERTER MODEL

Now, these steps could be exploited for modeling the PUC as a MCRS.

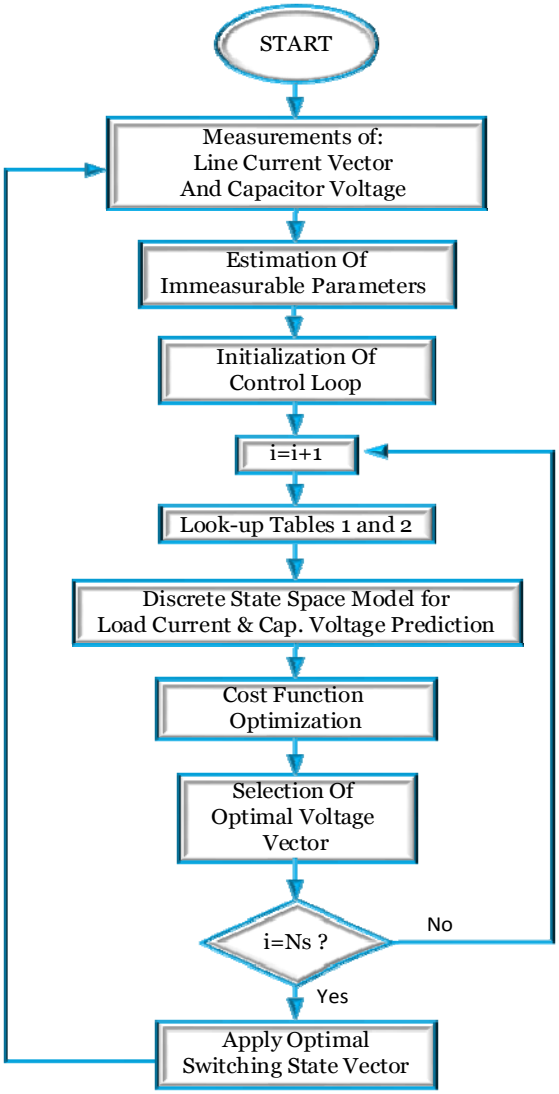


Figure 1. Flow diagram of the predictive control for a typical MCRS (N_s is the number of switching state vectors).

3.1. Modeling of PUC

A single-phase packed U-cell converter with connected active load is considered in [13]. Here the single-phase configuration is extended to three-phase converter, as depicted in Figure 2, which is composed of 18 power switches, three principal DC-link capacitors as well as three auxiliary DC-link. For three-phase configuration, there are 512 (8^3) switching states. The voltage in any phase of the inverter is expressed based on switching states and capacitor voltages (principal and auxiliary DC link) as the following (Based on switching table illustrated in [13]):

$$\left[v_{jn}\right]_{3\times1} = \left[S_{1j} - S_{2j} \quad S_{2j} - S_{3j}\right]_{3\times2} \begin{bmatrix} v_{c1j} \\ v_{c2j} \end{bmatrix}_{2\times3} \tag{9}$$

where v_{jn} $(j = a, b, c)$ is the phase to neutral voltages of the converter (j-phase). Also, v_{c1j} and v_{c2j} are the principal (C_1) and auxiliary (C_2) DC-link voltage, respectively.

While the single-phase PUC introduces 7 different voltage levels, the extended three-phase configuration provides 13-levels for line voltage and 7-levels for converter phase to neutral (n) voltage.

Based on Eq. (9), the derivative of load current in any phase-j of the converter can be written as:

$$L\frac{di_j}{dt} = -E_j - \mathrm{R}i_j + \left(S_{1\mathrm{j}} - S_{2\mathrm{j}}\right)v_{c1\mathrm{j}} + \left(S_{2\mathrm{j}} - S_{3\mathrm{j}}\right)v_{c2\mathrm{j}} \tag{10}$$

where L is the load inductance, R the load resistance, C_1 and C_2 are the principal and auxiliary DC-link capacitors, and E_j is the internal voltage vector of the load for phase j.

By considering the inverter output voltage vector as Eq. (11), there are 512 voltage vectors in inverter output, based on 512 switching states.

$$\boldsymbol{v}_{ref} = \frac{2}{3}(v_{an} + a.v_{bn} + a^2.v_{cn}) \quad , \quad a = e^{j\frac{2\pi}{3}} \tag{11}$$

The equations of a general load for each phase (as depicted in Figure 2) can be written as:

$$v_{jn} = L\frac{di_j}{dt} + Ri_j + E_j + v_{Nn} \tag{12}$$

where v_{Nn} is the voltage between load and converter neutral points.

According to [17], and substituting (12) into (11), the dynamic behavior of a general load can be described by,

$$\boldsymbol{v} = R\boldsymbol{i} + L\frac{d\boldsymbol{i}}{dt} + \boldsymbol{e} \tag{13}$$

where $\boldsymbol{v}$ is vector of the converter output voltage, $\boldsymbol{i}$ is the load current vector, and $\boldsymbol{e}$ the internal voltage vector of the load.

By considering vector presentation, three phase space voltage vector $\boldsymbol{v}$ is as follows:

$$\boldsymbol{v} = \boldsymbol{S}_1 v_{c1} + (v_{c2} - v_{c1})\boldsymbol{S}_2 - \boldsymbol{S}_3 v_{c2} \tag{14}$$

where $\boldsymbol{S}_1 = [S_{1a}, S_{1b}, S_{1c}]^T$, $\boldsymbol{S}_2 = [S_{2a}, S_{2b}, S_{2c}]^T$, and $\boldsymbol{S}_3 = [S_{3a}, S_{3b}, S_{3c}]^T$.

The capacitor voltages are expressed based on capacitor currents as follows:

$$\frac{dv_{ci}(t)}{dt} = \frac{1}{c}i_{ci}(t) \quad , \quad i = 1, 2 \tag{15}$$

The principal DC link capacitor currents (i.e.,i_{c1_a},i_{c1_b}, and i_{c1_c}) are predicted based on the three-phase load currents (i.e., i_a, i_b, and i_c) as follows:

$$i_{c1_j} = \left(S_{1j} - S_{2j}\right)i_j \tag{16}$$

Also, the auxiliary capacitor currents (i.e.,i_{c2_a},i_{c2_b}, and i_{c2_c}) are predicted as follows:

$$i_{c2_j} = \left(S_{2j} - S_{3j}\right)i_j \tag{17}$$

Based on equations (10), (16) and (17), the load currents and the capacitor voltages can be controlled by choosing a proper switching state vector.

3.2. Discrete Model for Prediction

The discrete model will be used to predict the future value of control parameters at time instant of $(k+1)th$. The load current derivative $\frac{d\boldsymbol{i}}{dt}$ is replaced by (Euler approximation),

$$\frac{d\boldsymbol{i}}{dt} \approx \frac{\boldsymbol{i}(k+1) - \boldsymbol{i}(k)}{T_s} \tag{18}$$

where T_s is the sampling period. According to Eq. (13), by using Euler approximation, the expression for prediction of future load current is (ideal case) [17]:

$$\boldsymbol{i}^{p}(k+1)=\left(1-\frac{RT_s}{L}\right)\boldsymbol{i}(k)+\frac{T_s}{L}\left(\boldsymbol{v}(k)-\hat{\boldsymbol{e}}(k)\right) \tag{19}$$

where $\hat{\boldsymbol{e}}$ denotes the estimated internal voltage vector of the load and $\boldsymbol{v}(k)$ is the output voltage vector of the inverter.

The estimated internal voltage vector of the load is calculated through the following formula [16]:

$$\hat{\boldsymbol{e}}(k-1)=\boldsymbol{v}(k-1)-\frac{L}{T_s}\boldsymbol{i}(k)-\left(R-\frac{L}{T_s}\right)\boldsymbol{i}(k-1) \tag{20}$$

The frequency of the internal voltage vector (back-EMF) of the load is much less than the sampling frequency. In this paper, the sampling frequency used with the FCS-MPC strategy was $10\,kHz$. So, for simplicity of calculations, the variations of $\boldsymbol{e}$ can be neglected in one sampling interval; thus: $\hat{e}(k)=\hat{e}(k-1)$. Although, this approximation is not valid when the sampling frequency is low.

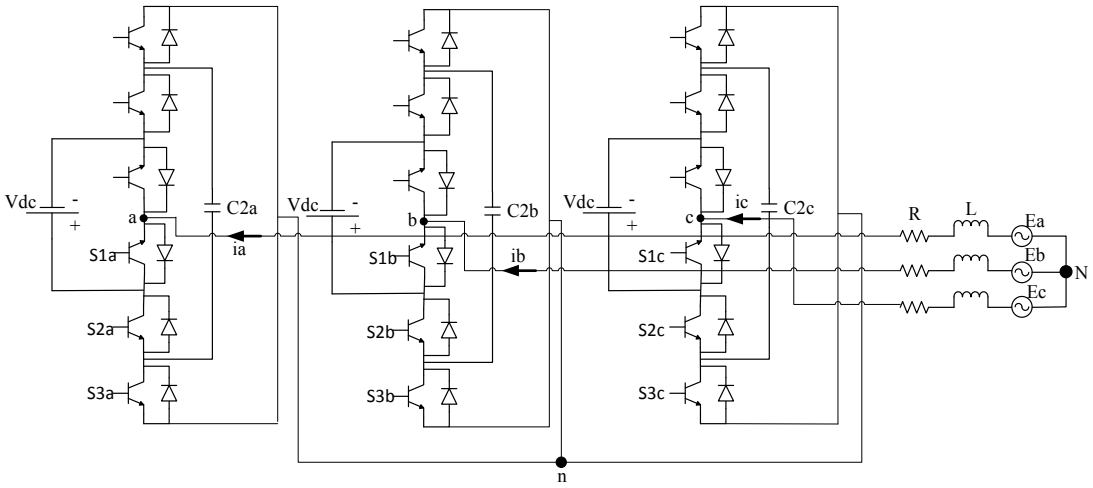


Figure 2. Suggested configuration for 7-level three-phase PUC ($v_{c1}=V_{dc}$).

According to Eq. (15) and using Euler approximation, the expression for prediction of future capacitor voltage is (ideal case):

$$v_c(k+1)=v_c(k)+\frac{T_s}{c}i_c(k) \tag{21}$$

where $v_c(k)$ is the measured voltage of the capacitor and $i_c(k)$ calculated based on Eqs. (16) and (17).

3.3. Two-Step-Ahead Prediction

The ideal case in which the control parameters can be measured, predicted, and controlled instantly in $t = t_k$ is impossible in real-time applications. Nonetheless, this problem can be can be overcome if a two-step-ahead prediction is considered. This way, a complete sample period T_s is available to perform the control algorithms [14]. Thus, equations (19) and (21) can be modified as follows:

$$\boldsymbol{i}^{p}(k+2)=\left(1-\frac{RT_s}{L}\right)\boldsymbol{i}^{p}(k+1)+\frac{T_s}{L}\left(\boldsymbol{v}(k+1)-\hat{\boldsymbol{e}}(k+1)\right) \tag{22}$$

$$v_c(k+2)=v_c(k+1)+\frac{T_s}{c}i_c(k+1) \tag{23}$$

The future reference currents are obtained by [24] (for highly dynamic systems),

$$i_{ref}(k+2)=10i_{ref}(k)-20i_{ref}(k-1)+15i_{ref}(k-2)-i_{ref}(k-3) \tag{24}$$

4. FCS-MPC

4.1. Control Strategy

The proposed predictive control strategy is developed in a way to track the reference load currents and regulate the capacitor voltages. For this purpose, it is necessary to measure the three-phase load currents

and voltages in the capacitors, predict the state space variables and evaluate a cost function g for each switching states. The switching state that minimizes the cost function is selected and applied during the next sampling period. Proposed FCS-MPC control scheme for a three-phase 7-level PUC converter is shown in Figure 3. Here 512 switching vectors at the kth sampling time are used to predict the converter output voltage. The prediction of load currents and DC-link capacitor voltage are done using (22) and (23).

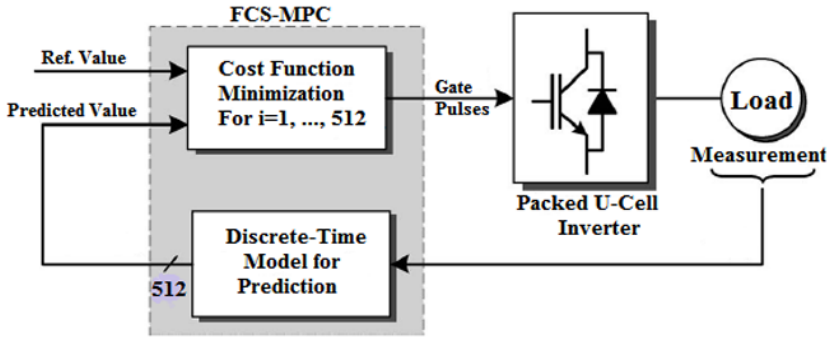


Figure 3. FCS-MPC for three-phase PUC converter.

4.2. Cost Function

Based on the control requirements (load current reference tracking and auxiliary capacitor voltage balance), the cost function to be optimized, is represented at the kth sampling time as follows [17]:

$$g = \left| \boldsymbol{i}^{*}_{real}(k+1) - \boldsymbol{i}^{p}_{real}(k+1) \right| + \left| \boldsymbol{i}^{*}_{imag}(k+1) - \boldsymbol{i}^{p}_{imag}(k+1) \right| + w_1 \sum_{i=a,b,c} \left| \frac{V_{dc}}{n} - v_{c_i} \right| + w_2 N_c \quad (25)$$

where $\boldsymbol{i}^{*}_{real}$, and $\boldsymbol{i}^{*}_{imag}$, are the real and imaginary parts of reference currents, respectively. The $\boldsymbol{i}^{p}_{real}$, and $\boldsymbol{i}^{p}_{imag}$ are predicted currents, w_1 and w_2 are weighting factors.

The last term is the number of commutations (N_c) required to change from the present switching vector to the future switching state vector. By using this term, the switching frequency of the converter can be decreased. Each term in the cost function has a specific weighting factor which is used to tune the importance of that term in relation to the others control targets. These parameters have to be properly designed in order to achieve the desired performance. Unfortunately, there are no analytical or numerical methods or control design theories to adjust these parameters [25]. In this paper, the procedure to determine the weighting factor is based on the empirical method. In [26] a clear and objective method is used to select an appropriate weight factor range.

5. SIMULATIONS

To verify the flexibility of the proposed control technique, a power circuit was simulated in MATLAB /SIMULINK. The system consists of a three-phase PUC converter, load, and control units (predictive controller). The sampling frequency used with the predictive strategy was 10 kHz. For steady state condition in the simulated system, only 238 switching state vectors among 512 possible states is used for synthesizing inverter output voltage. As a result, lots of switching state in look-up table can be removed and the computational burden is decreased. In general, a specific switching state vector can be removed from look-up table depending on:

1. Transient or steady state operation mode of the inverter.
2. Number of control parameters that included in the cost function.
3. Value of weighting factors.

5.1. Steady-State Performance

Figure 4 shows that the load currents tracks reference values, accurately, and its THD is less than 1%. Negative cycle of principal DC-link current as shown in Figure 4, indicates that bidirectional power supply is needed (because of trinary mode, namely capacitor voltage is equal to $V_{dc} = v_{c1} = 3v_{c2}$). More voltage levels and low THD is obtained in trinary case, but it is harmful for DC-link power supply (or battery). This problem can be removed by using $V_{dc} = v_{c1} = 2v_{c2}$ (binary case).

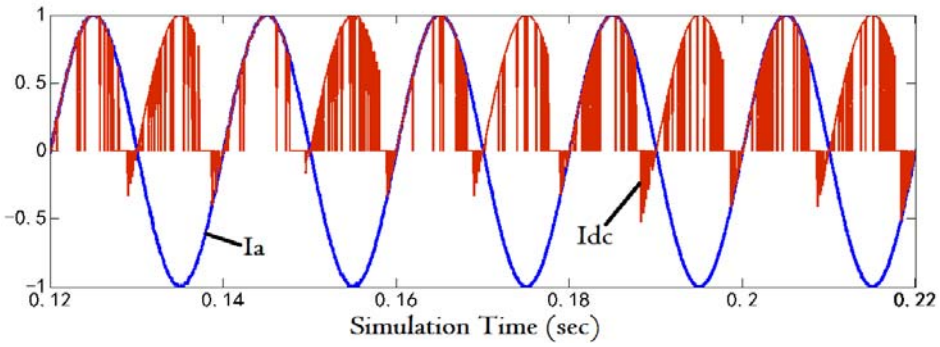


Figure 4. Three-phase load currents i_{abc} (p. u.), and principal DC-link current $i_{c1} = i_{dc}$ (p. u.).

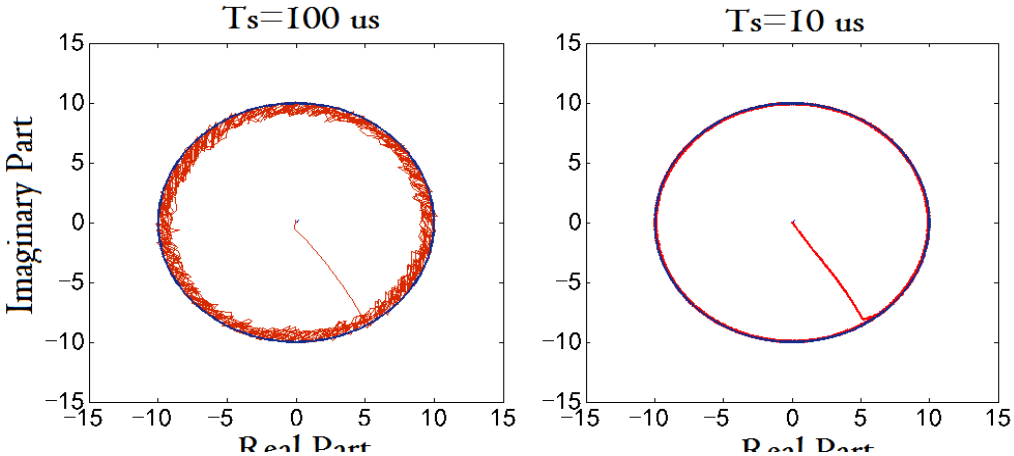


Figure 5. Sampling time effect on reference current tracking of phase a (per unit value).

Real and imaginary parts of the predicted load currents (red) and their references (blue) are shown in Figure 5 (vertical plot). Figure 5 indicates the sampling frequency effect on reference current tracking. As it can be seen, more sampling frequency results in accurate reference current tracking (because of nature of predictive control), and low switching frequency cause a one sample delay in current tracking and increases output voltage THD [16].

Real and estimated internal voltage vector of the load are shown in Figure 6. Internal voltage vector of the load is estimated using Eq. (22) with a sampling time $T_s = 100\,\mu s$. Because of low order Euler approximation of current derivative and other assumptions, a low pass filter is required for better estimation of internal voltage vector of the load.

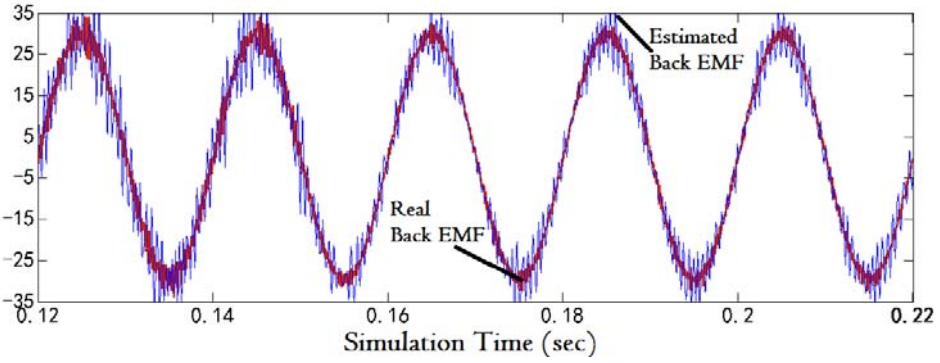


Figure 6. Estimated and real internal voltage vector of the load.

Figure 7 shows system voltages (phase-a) where 13-level in line-to-line voltage can be seen. Load and line-to-line voltage THDs, are 8.6% and 7.96%, respectively. THD decreases considerably as well as the increment in the number of output voltage levels and it's suitable for power quality applications. As far as simulation results indicate, the number of voltage levels is related to the capacitor voltage balancing gain (w_1). By increasing or decreasing w_1, the number of output voltage levels could be changed. This indicates that there is an indirect relationship between modulation index and the capacitor voltage balancing gain (or the number of output voltage levels).

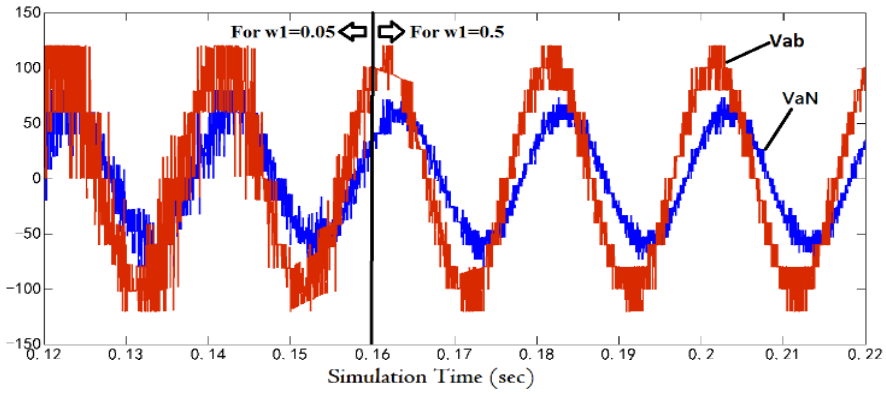


Figure 7. Line voltage (V_{ab}), and load voltage (V_{aN}).

As shown in Figure 8, before $t = 0.1\,s$, for $w_1 = 0.5$, the proposed method regulate capacitor voltage, and after $t = 0.1\,s$ with $w_1 = 0$, as expected, capacitor voltages quickly began to increase. So, the proposed control strategy succeeded in balancing auxiliary DC link capacitor voltage.

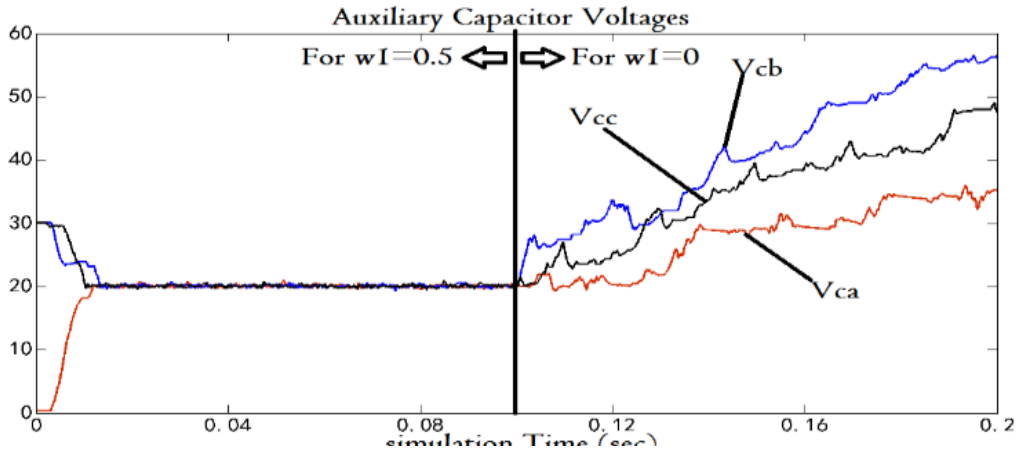


Figure 8. Effects of w_1 on capacitor voltage balancing.

5.2. Performance During transient

Dynamics performance of the FCS-MPC scheme was investigated, using SIMULINK and compared with a modified Level-shifted PWM (LS-PWM) control scheme that presented in [13].

For evaluation of reference current tracking, the reference of the load currents was changed from rated condition to zero at time-instant $t = 245\,ms$. At $t = 445\,ms$, the load current reference was changed back to rated value. As shown in Figure 9 and Figure 10, FCS-MPC achieves a very fast reference current tracking at both condition. It takes less than 3 ms to deliver the rated load currents. On the other hand, the LS-PWM scheme provides a slow response. Figure 10 shows that the load currents overshoot before settling at their steady state values. With LS-PWM technique, the reference current tracking might not be further improved because of PI gains limitations that will result in oscillations in the load currents.

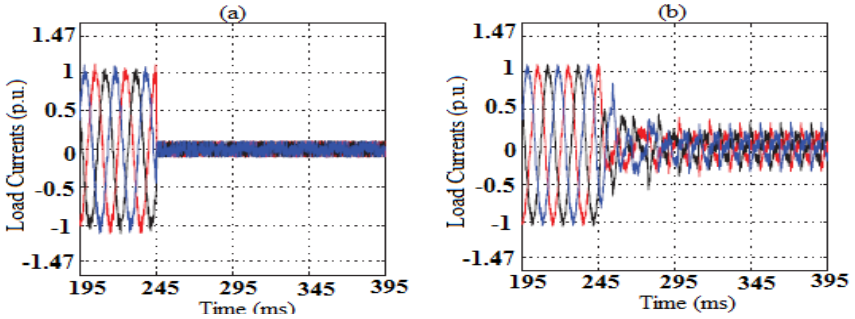


Figure 9. Load currents during the power-down transient, (a) FCS-MPC, and (b) LS-PWM.

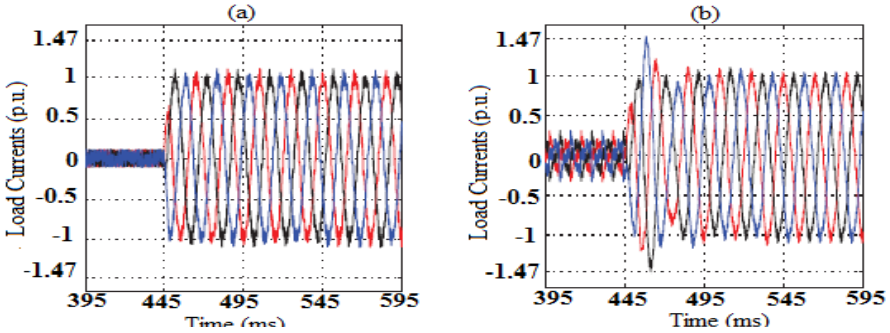


Figure 10. Load currents during the power-up transient, (a) FCS-MPC, and (b) LSP-WM.

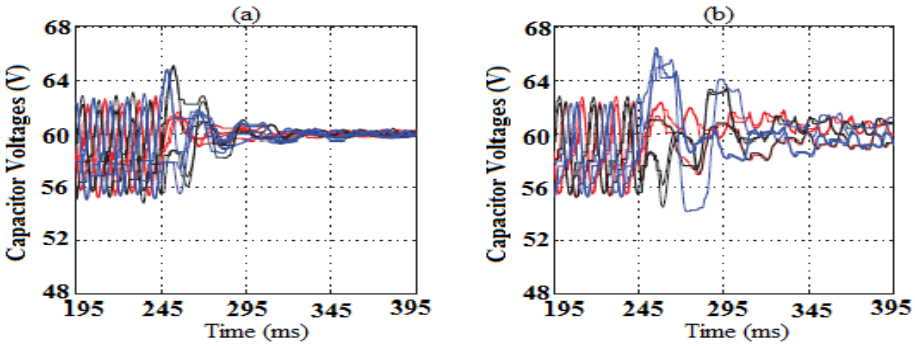


Figure 11. Capacitor voltages during the power-down transient, (a) FCS-MPC, and (b) LS-PWM.

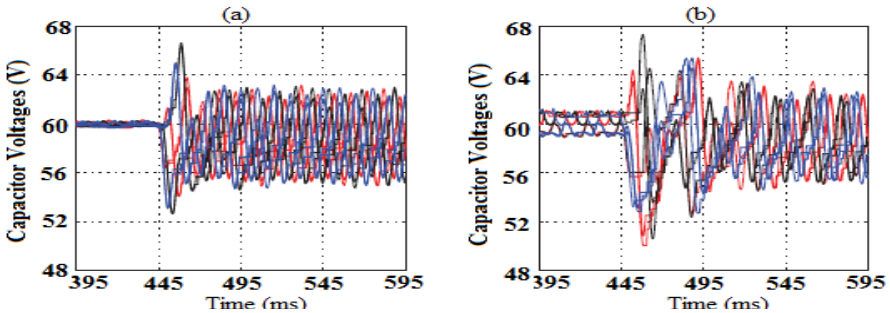


Figure 12. Capacitor voltages during the power-up transient, (a) FCS-MPC, and (b) LS-PWM.

With the FCS-MPC scheme, the capacitor voltages, as shown in Figure 11 and Figure 12, are well regulated at both condition. After power-up, the capacitor voltages settle within 5% of the average voltage value in less than three fundamental cycles. Whereas, with the LS-PWM scheme, the capacitor voltages show large oscillations.

5.3. Performance Evaluation

One of the prime requirements in high power converters to be provided for effective operation, is the ability to operate with lower switching frequency and optimum THD. Although there are various redundant switching states that are able to provide the same line voltage in the output side of a multi-level converter, the most efficient states should be chosen to reduce switching frequency. For reducing switching frequency, every instant, the switching state that reduces the number of commutations (N_c) should be chosen. For measuring the effect of control algorithm on switching frequency and reference tracking, the average switching frequency per semiconductor f_s and reference current tracking error $\bar{e}$ can be calculated [16].

Figure 13 shows the relation between average switching frequency (f_s) and reference tracking error of load current ($\bar{e}$) with w_2. The maximum allowable value for w_2 is 0.015, because of maximum absolute current error and minimum switching frequency that is required for optimum performance of the system.

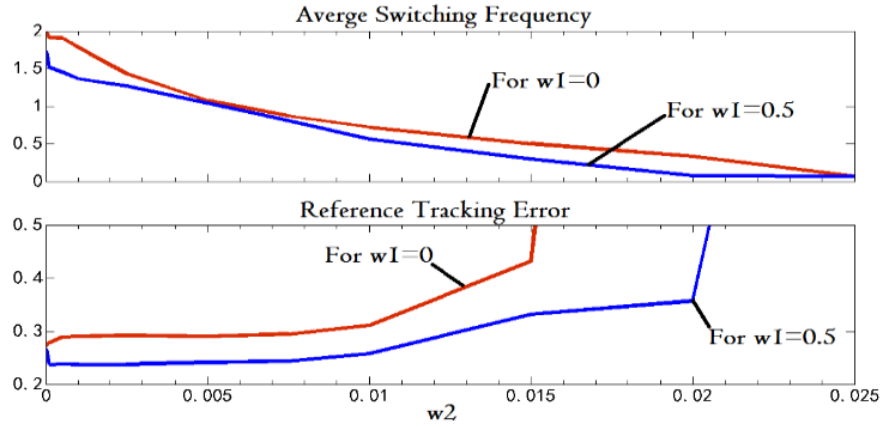


Figure 13. Parameter w_2, (a) relation with the average switching frequency [kHz], and (b) relation with the reference current tracking error [A].

Table 1 shows the relation between w_1 and w_2 with THD of line voltage V_{ab}. As it can be seen, for $w_1 = 0.5$ and $w_2 = 0.01$, control system has good performance.

Table 1 Relation Between w_1, w_2 and Line Voltage THD

	THD of Line Voltage V_{ab} (%)				
w1	w2=0	w2=0.001	w2=0.01	w2=0.015	w2=0.02
0.001	13.35	13.07	18.68	22.21	49.75
0.01	12.88	16.56	14.97	20.14	49.45
0.1	7.33	11.78	13.36	17.86	49.45
0.5	9.96	9.89	10.28	14.36	18.36
1	14.58	14.3	15.14	21.79	21.81
10	19.06	17.58	21.17	19.95	24.59
100	24.69	22.55	22.41	20.77	24.71

6. EXPRIMENTAL RESULTS

MATLAB/ SIMULINK environment is used for the design and off-line simulation of the models and power electronic circuits. The Real Time Workshop converts the Simulink model to C programming code. In order to support the theory and validate simulation results, a 5 kVA prototype was implemented as shown in Figure 14. The exploited switches are 1200 V, 42 A of IGBT type BUP314D. The eZdsp TMS320 F28335 board is employed to control the processes (e.g., load current and capacitor voltage prediction, and cost function optimization).

Load currents and the capacitor voltages are measured using ACS712 sensor and LV25-P transducer, respectively. To observe the current waveforms GW INSTEK GCP-100 current probe was utilized (each 100 mV equal to 1 Amp). The predictive controller generates the gating signals to be sent to the converter through the gate driver circuits. The experimental results are obtained during the steady states with balanced load considering a sampling time of $T_s = 100\ \mu s$. Complete list of different elements in both

simulation and experimental condition are provided in Table 2. In the experimental setup (as depicted in Figure 14), a three-phase induction motor was utilized.

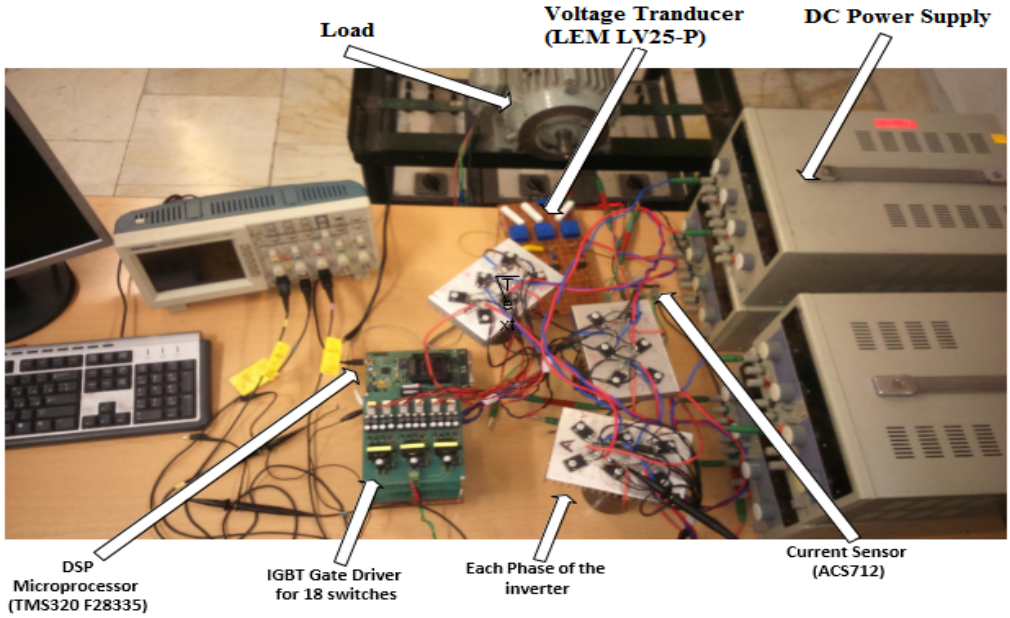
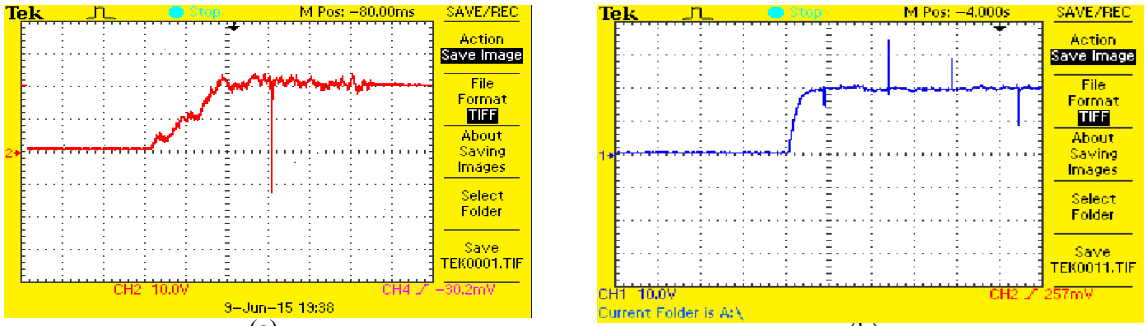


Figure 14. The laboratory 5kVA prototype, which is controlled under model based predictive principles.

The capacitor voltage is shown in Figure 15 (in this case, principal DC-link is 60 volts). By applying the proposed control technique, the capacitor is charged. As shown in Figure 13(b), by increasing the capacitor voltage balancing weighting factor (w_1), rise time and ripple of capacitor voltage is improved. These results are in agreement with those of simulations.



(a) (b)

Figure 15. Experimental results of capacitor voltage balancing during steady state with balanced active RL load, capacitor voltage (v_{ca}) ($10\ V/div$,$0.5\ sec/div$) with, (a) $w_1 = 0.05$ ($v_{ripple} = 5V$), (b) $w_1 = 0.5$ ($v_{ripple} = 1V$).

As shown in Figure 16, there are 13 voltage levels at output side of the inverter (line voltage v_{ab}, with three phase active load) that proves the ability of the proposed control scheme in producing a voltage with low THD, since the more number of levels, the less THD (for better resolution on voltage steps, principal DC-link is 100 volts). The average switching frequency f_s is about 2000 Hz.

Figure 17(a) indicates the current waveform in extended form and effects of weighting factor on steady state performance. As can be seen, the current of the load is almost a pure sinusoidal and has acceptable THD. The performance index parameters (i.e., $\bar{e}$ and total harmonic distortion (THD)) are calculated. For optimum value of the capacitor voltage balancing weighting factor in the cost function ($w_1 = 0.5$), this approach produces 6% reference tracking error and 4.8% THD. Consequently, for balanced reference, the load current regulation is obtained (A balanced reference of 1 A is considered).

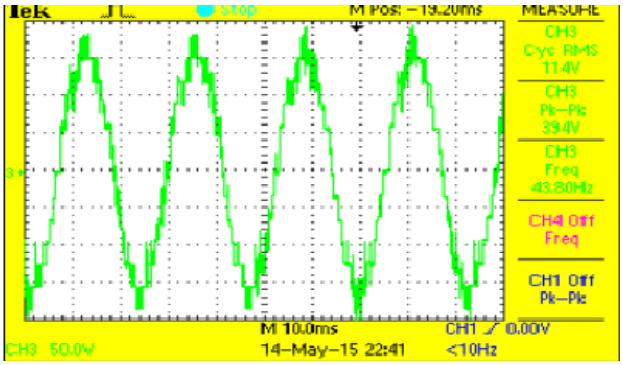
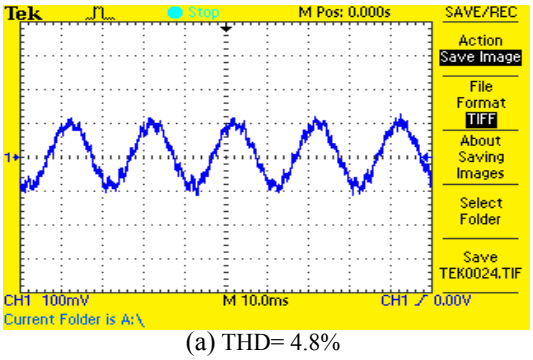
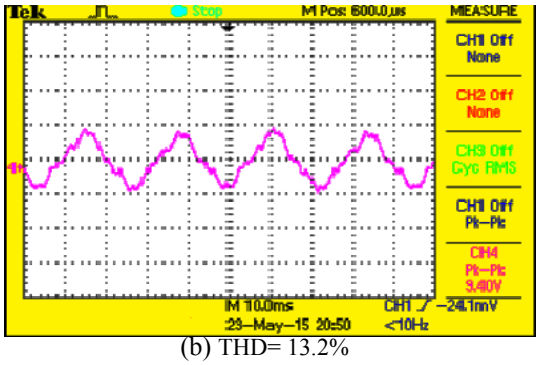


Figure 16. Line voltage v_{ab} for $V_{dc} = 100\,Volts$ $(50\,V/div)$.



(a) THD= 4.8%



(b) THD= 13.2%

Figure 17. Load currents with, (a) $w_1 = 0.5$, and (b) $w_1 = 0.05$ (1 A/div, 0.01 Sec/div).

Figure 18 indicates, when the control scheme is applied to the inverter, capacitor balancing initiates and the voltages across the capacitor tracks the reference value (20 volts). This figure includes the load current which is shown simultaneously with capacitor voltage.

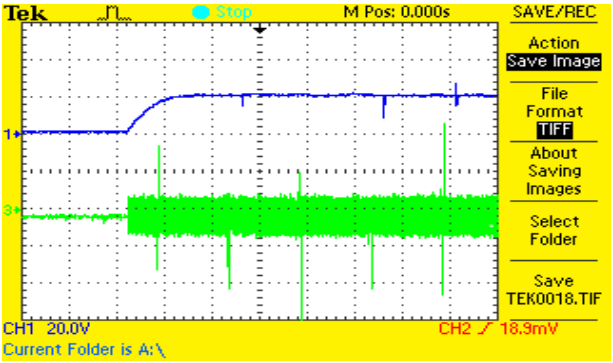


Figure 18. Capacitor voltage and load current at control initialization $(20\,V/div\,, 2\,A/div)$.

Table 2 Experimental and Simulation Parameters

Variable	Description	Value
C_{dc}	DC-link capacitance	4700 μF
L	Load inductance	15 mH
R	Load resistance	5.6 Ω
f_s	Sampling frequency	10 kHz
V_{dc}	DC-link nominal voltage	60 and 100 V
i^*	Nominal reference load current	1A
w_1	Capacitor weighting factor	0.5

7. CONCLUSION

This paper proposes a finite control set MPC strategy to control a three-phase reduced structure multilevel converter. A case study considered, the packed U-cell, which is among reduced structure multilevel converters. A 5 kVA packed U-cell was implemented to experiment both predictive control effects and capacitor voltage balancing approach. According to the reference current tracking error ($\bar{e}$), load currents are tracked to their references with an acceptable error. The DC-link capacitor voltages are balanced during steady state operating conditions. For a given sampling time T_s, load currents have an acceptable quality with lower average switching frequency (lower average power losses) and THD for load current (below 5%).

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